

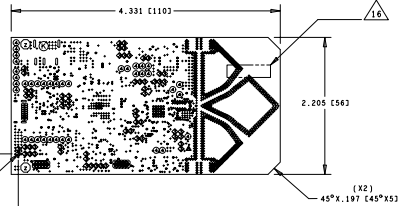
NOTES (UNLESS OTHERWISE SPECIFIED):

- THIS DRAWING SPECIFIES THE REQUIREMENTS FOR A PRINTED WIRING BOARD IN ACCORDANCE WITH SPECIFICATION IPC-6012 CLASS 2 (LATEST REVISION).
- THE PWB MUST BE LEAD FREE ASSEMBLY PROCESS COMPATIBLE AND MUST BE ABLE TO HANDLE A MINIMUM OF 5 CYCLES AT 260 DEGREES CELSIUS FOR 10 SECONDS.
- BASE MATERIAL - LAMINATE AND PREPREG SHALL MEET IPC-4101D-26, B3 or B8  
Tg - MUST BE GREATER THAN OR EQUAL TO 150 DEGREES CELSIUS.  
Td - MUST BE GREATER THAN OR EQUAL TO 330 DEGREES CELSIUS.
- COPPER FOIL WEIGHT - SEE STACKUP DETAIL 'A'
- CHARACTERISTIC IMPEDANCE - SEE DETAIL 'B'
- MINIMUM CONDUCTIVE WIDTH/SPACING TO BE .004"/.0044"
- PLATING FINISH: A. IMMERSION GOLD: 2-8 MICROINCHES OF GOLD OVER 100-250 MICROINCHES MINIMUM NICKEL.
- FAB VENDOR IS NOT ALLOWED TO USE ODB FOR FABRICATION. CAN BE USED ONLY FOR REFERENCE.
- SOLDERMASK - TO MEET THE REQUIREMENTS OF IPC-SM-840E (OR LATEST REVISION). GREEN COLOR, BOTH SIDES. MODIFICATION OF SOLDERMASK IS NOT ALLOWED WITHOUT WRITTEN PERMISSION FROM NXP. TYPE: LPI OR EQUIVALENT.  
A. LOCATION +/- .002" OF PLATED PADS.  
B. DIAMETER OR SIZE +/- .002 OF ORIGINAL DATA
- SILKSCREEN - WHITE EPOXY OR ACRYLIC INK, BOTH SIDES. NO SILKSCREEN ON ANY EXPOSED COPPER FEATURE.
- ELECTRICAL TEST - 100% IPCD356. PCB FABRICATOR TO PERFORM A NET COMPARE AGAINST THE IPCD356 NETLIST PROVIDED BY NXP.
- PRINTED WIRING BOARD IS TO BE INDIVIDUALLY BAGGED.
- DFM CHECK MUST BE RUN ON BOARD DATA BEFORE BUILDING BOARDS. UNLESS PRIOR APPROVAL IS GIVEN IN WRITING BY NXP.
- TEARDROPS MAY BE ADDED AT THE FAB HOUSE TO ALL SIGNAL LAYERS.
- TWO SOLDER SAMPLES TO BE PROVIDED.
- SUPPLIER MARKINGS - ON SECONDARY SIDE ONLY, WHERE SHOWN.  
- MUST BE UL RECOGNIZED AND MUST HAVE AN ID THAT CONFORMS TO UL94V-0
- THE PWB WILL BE MARKED AS LEAD FREE BY USE OF AN INK STAMP (26)
- THE PWB WILL BE MARKED AS LEAD FREE PROCESS COMPATIBLE BY USE OF AN INK STAMP (260)
- ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP. ALL HOLE LOCATION TOLERANCES ARE TO BE +/- .002 IN REFERENCE TO THE PRIMARY DATUM UNLESS OTHERWISE SPECIFIED.
- FINISHED PCB MUST BE PANELIZED FOR ASSEMBLY ACCORDING TO CONTRACT MANUFACTURERS REQUIREMENTS. THE ADDITION OF RAILS AND .125" NON-PLATED TOOLING HOLES ARE AT THE DISCRETION OF CONTRACT MANUFACTURER. PANELIZATION MUST BE APPROVED BY CONTRACT MANUFACTURER.
- THE MANUFACTURE HAS THE OPTION TO ADD COPPER THIEVING ON OUTER AND INNER LAYERS. KEEP A MINIMUM DISTANCE OF .100" FROM ANY BOARD FEATURES.
- THIS BOARD USES VIA-IN-PAD: SEE FAB\_VIAFILL.AT  
A. ALL VIAS USING X.1 DRILL SIZES ARE TO BE FILLED WITH NON-CONDUCTIVE VIA FILL. LACKWERKE-PETERS PP2795 OR EQUIVALENT AND MADE PLANAR TO THE PADS.  
B. OVERPLATE THE FILLED VIA AND APPLY FINISH METAL TREATMENT.  
C. DIMPLE ON VIA-IN-PADS MUST BE NO GREATER THAN .003" AND PROTRUSION NO GREATER THAN .002"

23. INTENTIONAL 29 SHORTS AT:

LocationStart	LocationEnd	RefDes	Net 1	Net 2
(210.00 303.00)	(210.00 343.00)	SH1	RESET	RST_TOTMCU_B
(110.00 303.00)	(110.00 343.00)	SH2	AN	ADC_IN
(131.26 936.26)	(131.26 1015.00)	J55	UART_RX	UART_RX
(210.00 1015.00)	(210.00 936.26)	J56	UART_TX	UART_TX
(66.00 980.00)	(66.00 1020.00)	SH3	PTD2/TMP1_CHO	PWM
(97.24 1301.26)	(97.24 1380.00)	J54	PSV_CAN	FL_USB_SVO
(310.00 303.00)	(310.00 343.00)	SH4	SPI_PCSO	LPSP1_PCSO
(410.00 303.00)	(410.00 343.00)	SH6	SPI_SCK	LPSP1_SCK
(470.00 1060.00)	(510.00 1060.00)	SH11	I2C1_SCL	I2C_SCL
(295.00 1060.00)	(335.00 1060.00)	SH5	WU0_P12/NM1_B	LLWU/NM1_B
(482.80 31.26)	(482.80 110.00)	J52	P_LED	V_BRD
(610.00 303.00)	(610.00 343.00)	SH10	SPI_SOUT	LPSP1_SOUT
(510.00 303.00)	(510.00 343.00)	SH8	SPI_SIN	LPSP1_SIN
(570.00 1060.00)	(610.00 1060.00)	SH13	PTD3/I2C1_SDA	I2C_SDA
(710.00 300.00)	(710.00 340.00)	SH12	SV3_MIKROE	V_BRD
(750.00 1060.00)	(710.00 1060.00)	SH14	PSV	SV_MIKROE
(1095.71 -2.04)	(1095.71 -80.78)	J514	TMP1_CHO	LED1_B1
(1498.86 1619.02)	(1498.86 1682.02)	SH19	P3V3_LDO	V_BRD
(1802.41 505.00)	(1782.41 505.00)	SH15	V_BRD	VCC_TGMCU
(1782.74 1781.74)	(1782.74 1741.74)	SH21	VDD_IC	P_VDD_SWITCH
(1849.10 -7.06)	(1849.10 55.94)	SH20	BOOT_CFG	SNO/BOOT_CFG
(2094.30 1414.97)	(1994.30 1414.97)	J511	UART1_TX	N23938761
(2094.30 1289.97)	(1994.30 1289.97)	J510	UART1_RX	N23938720
(2094.30 1539.97)	(2015.56 1539.97)	J51	VDD_MEM	V_BRD
(2454.01 318.43)	(2454.01 358.43)	SH22	N24374306	VDD_DCDC
(2445.41 1289.97)	(2485.41 1289.97)	SH23	N24374396	VDD_RF
(2620.82 80.95)	(2620.82 159.69)	J53	RST_TOTMCU_B	LED_R15
(2872.48 922.47)	(2732.48 922.47)	SH24	RF_GPO_5	N24516334
(2722.41 424.47)	(2722.41 484.47)	SH9	RF_GPO_4	N24441947

PRIMARY DATUM  
GRID ORIGIN



DETAIL B  
IMPEDANCE REQUIREMENTS  
IMPEDANCE TOLERANCE IS 10%

SE				DIFF				COPLANAR			
LAYERS	TRACE WIDTH	IMPEDANCE	TRACE WIDTH	TRACE SPACING	IMPEDANCE	REFERENCE LAYER	TRACE WIDTH	TRACE SPACING	IMPEDANCE	REFERENCE LAYER	TRACE WIDTH
L1_P5	N/A	N/A	8.96	5.04	90.00	2	7.80	6.20	100.00	2	16.43
L3_INT	N/A	N/A	N/A	N/A	N/A	N/A	5.82	8.38	100.00	2	N/A
L4_INT	N/A	N/A	N/A	N/A	N/A	N/A	5.82	8.38	100.00	5	N/A
L6_35	N/A	N/A	8.96	5.04	90.00	5	7.80	6.20	100.00	5	N/A

\*IMPEDANCE TABLE VALUES ARE BASED ON THE FAB VENDOR SUPPLIED STACK-UP  
IF ANY IMPEDANCE IS NOT FOUND ON A SPECIFIC LAYER, PLEASE IGNORE IT

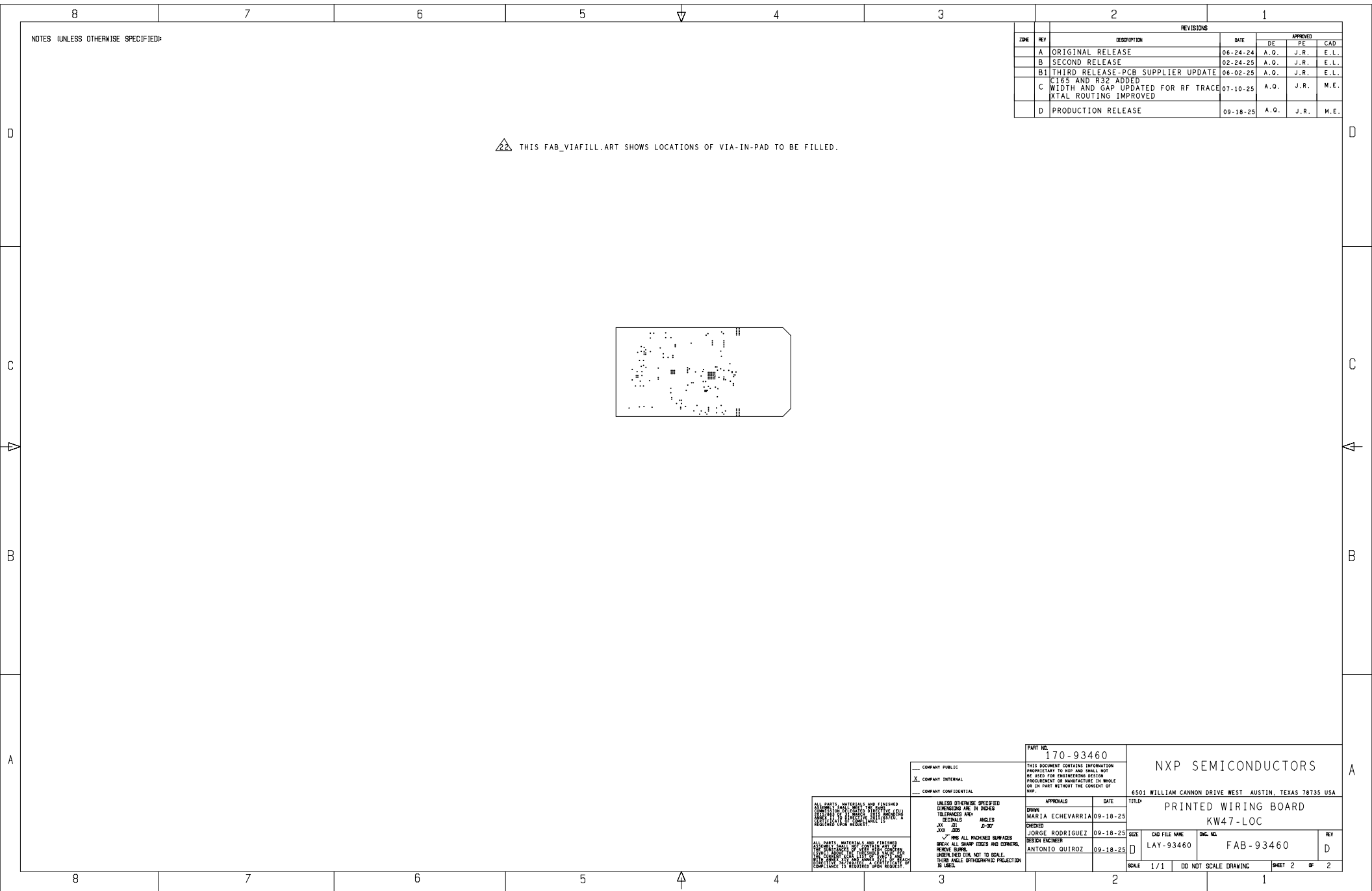
		REVISIONS		APPROVED	
ZONE	REV	DESCRIPTION	DATE	DE	CAD
	A	ORIGINAL RELEASE	06-24-24	A.O.	J.R.
	B	SECOND RELEASE	02-24-25	A.O.	J.R.
	B1	THIRD RELEASE-PCB SUPPLIER UPDATE	06-02-25	A.O.	J.R.
	C	C165 AND R32 ADDED WIDTH AND GAP UPDATED FOR RF TRACE XTAL ROUTING IMPROVED	07-10-25	A.O.	J.R.
	D	PRODUCTION RELEASE	09-18-25	A.O.	J.R.

L1	TOP CONDUCTOR - COPPER 1.83 MIL
	* DIELECTRIC - DRY FILM MASK 0.3 MIL
	* DIELECTRIC - IT-180ABS 10.16 MIL
L2	L2_GND_1 PLANE - COPPER 1.18 MIL
	* DIELECTRIC - IT-180ABS 10 MIL
L3	L3_INT_1 CONDUCTOR - COPPER 1.18 MIL
	* DIELECTRIC - IT-180ABS 9.6 MIL
L4	L4_INT_2 CONDUCTOR - COPPER 1.18 MIL
	* DIELECTRIC - IT-180ABS 10 MIL
L5	L5_GND_2 PLANE - COPPER 1.18 MIL
	* DIELECTRIC - IT-180ABS 10.16 MIL
L6	BOTTOM CONDUCTOR - COPPER 1.83 MIL
	* DIELECTRIC - DRY FILM MASK 0.3 MIL
	* SURFACE - AIR 0 MIL

DESIGN CROSS SECTION CHART  
TOTAL THICKNESS 58.9 MIL  
BOARD THICKNESS TOLERANCE +/-10%  
ALL VALUES ARE FINISHED VALUES  
DETAIL A  
LAYER STACKUP  
SCALE: NONE

DRILL CHART: TOP to BOTTOM				
ALL UNITS ARE IN MILS				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
+	8.0	+0.0/-8.0	PLATED	1488
⊙	8.1	+0.0/-8.1	PLATED	193
⊙	16.0	+2.0/-2.0	PLATED	16
⊙	28.0	+2.0/-2.0	PLATED	20
⊙	35.0	+2.0/-2.0	PLATED	5
⊙	35.0	+3.0/-3.0	PLATED	57
⊙	40.0	+2.0/-2.0	PLATED	8
⊙	40.0	+3.0/-3.0	PLATED	30
⊙	63.0	+3.0/-3.0	PLATED	1
⊙	100.0	+2.0/-2.0	NON-PLATED	1
⊙	118.0	+2.0/-2.0	NON-PLATED	2
⊙	55.0x24.0	+2.0/-2.0	PLATED	2
⊙	83.0x24.0	+2.0/-2.0	PLATED	2
⊙	111.0x32.0	+2.0/-2.0	PLATED	3
⊙	122.0x32.0	+2.0/-2.0	PLATED	2

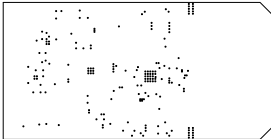
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APPROVALS		TITLE PRINTED WIRING BOARD KW47-LOC	
DATE		CNO FILE NAME LAY-93460	
DRAWN MARIA ECHEVARRIA		CNC NO. FAB-93460	
CHECKED JORGE RODRIGUEZ		REV D	
DESIGN ENGINEER ANTONIO QUIROZ		SCALE 1/1 DO NOT SCALE DRAWING	
SHEET 1 OF 2			



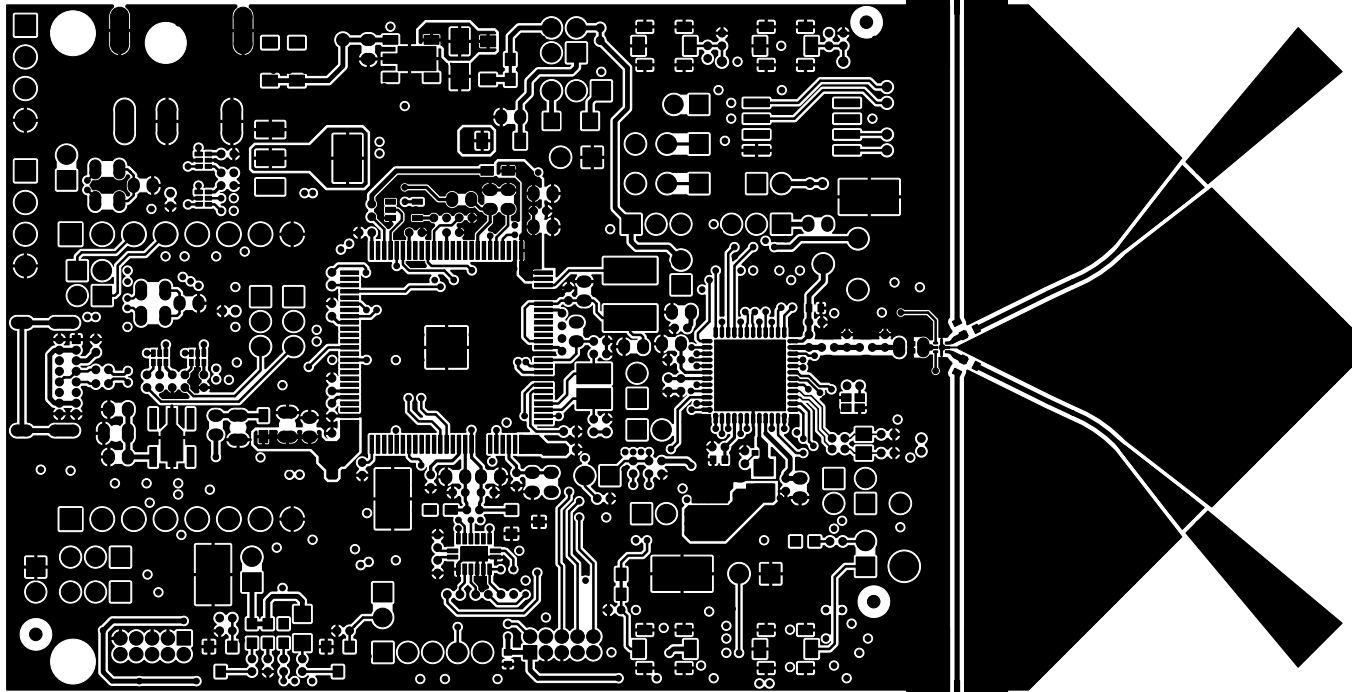
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	B	SECOND RELEASE	02-24-25	A.O.	J.R.	E.L.		
	B1	THIRD RELEASE-PCB SUPPLIER UPDATE	06-02-25	A.O.	J.R.	E.L.		
	C	C165 AND R32 ADDED WIDTH AND GAP UPDATED FOR RF TRACE XTAL ROUTING IMPROVED	07-10-25	A.Q.	J.R.	M.E.		
	D	PRODUCTION RELEASE	09-18-25	A.Q.	J.R.	M.E.		

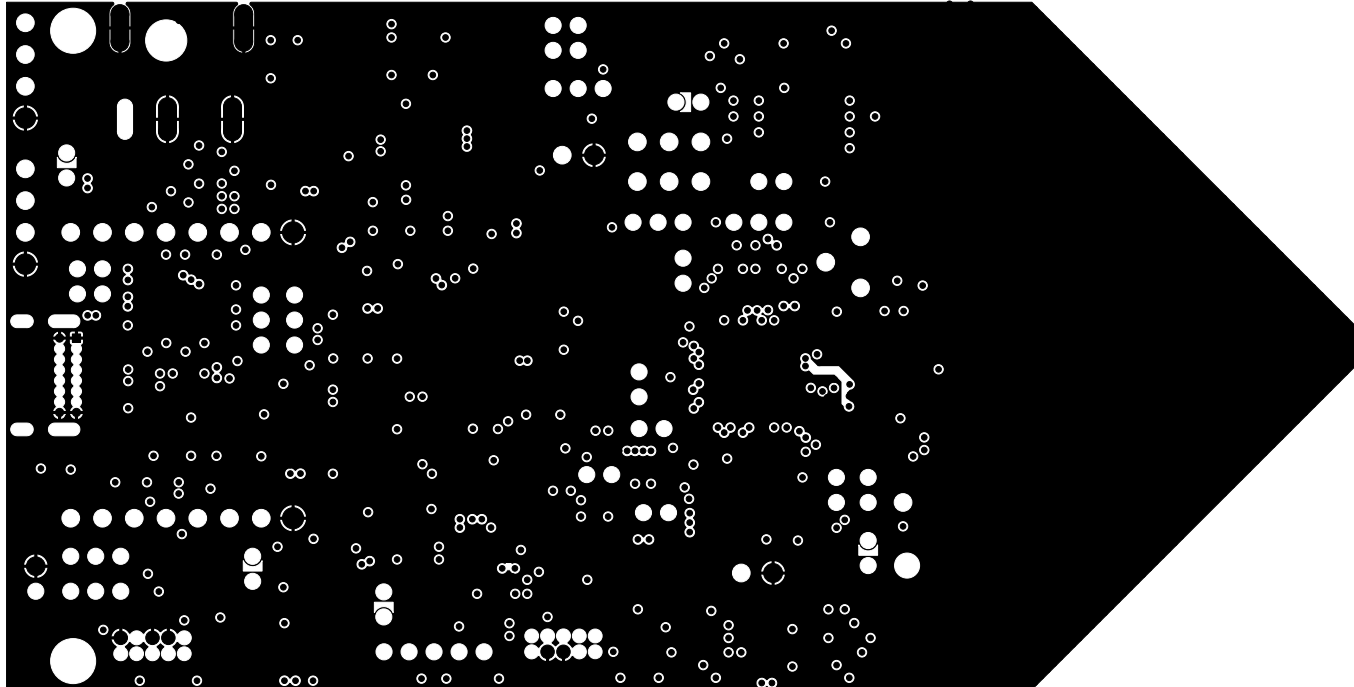
THIS FAB\_VIAFILL.ART SHOWS LOCATIONS OF VIA-IN-PAD TO BE FILLED.



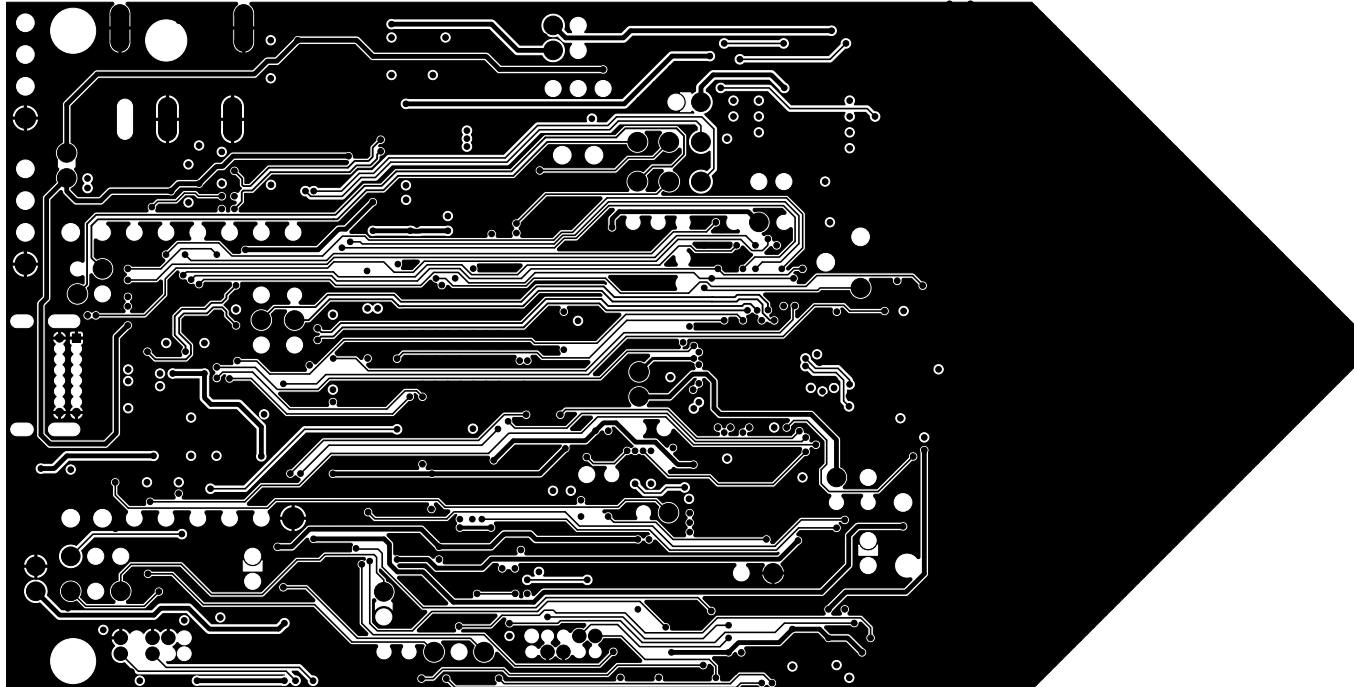
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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMALS XX .XX ANGLES 2-30° XXX .XXX		APPROVALS	DATE
DRAWN MARIA ECHEVARRIA		09-18-25	TITLE PRINTED WIRING BOARD KW47-LOC
CHECKED JORGE RODRIGUEZ		09-18-25	SIZE D
DESIGN ENGINEER ANTONIO QUIROZ		09-18-25	CAD FILE NAME LAY-93460
ALL PARTS, MATERIALS AND FINISHED PRODUCTS SHALL BE OF THE BEST QUALITY AVAILABLE AND SHALL BE SUBJECT TO THE REQUIREMENTS OF THE DRAWING. COMPLIANCE IS REQUIRED UPON REQUEST.		CNC NO. FAB-93460	
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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMALS XX .XX ANGLES 2-30° XXX .XXX		SCALE 1/1	
DO NOT SCALE DRAWING		SHEET 2 OF 2	



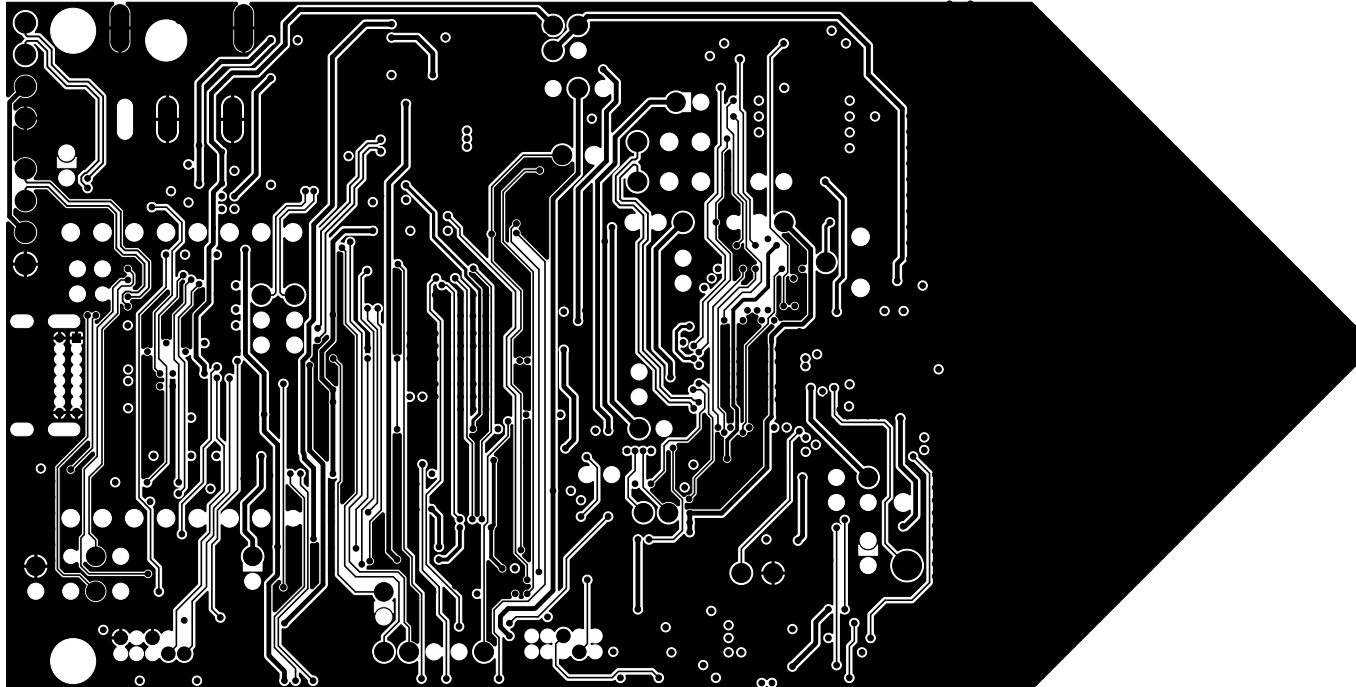
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SHEET 04 OF 12	FILM L1_PS	DATE 09-18-25	NUMBER 170-93460 REV D



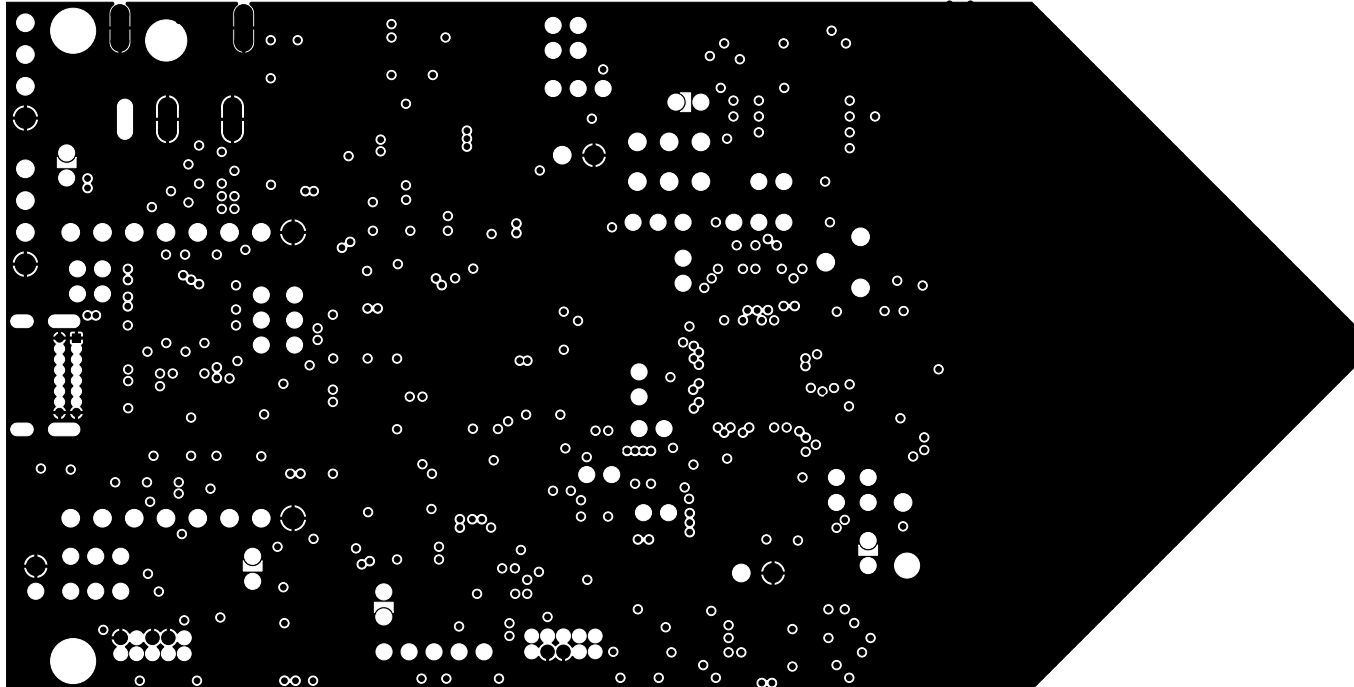
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SHEET 05 OF 12	FILM L2_GND_1	DATE 09-18-25	NUMBER 170-93460 REV D



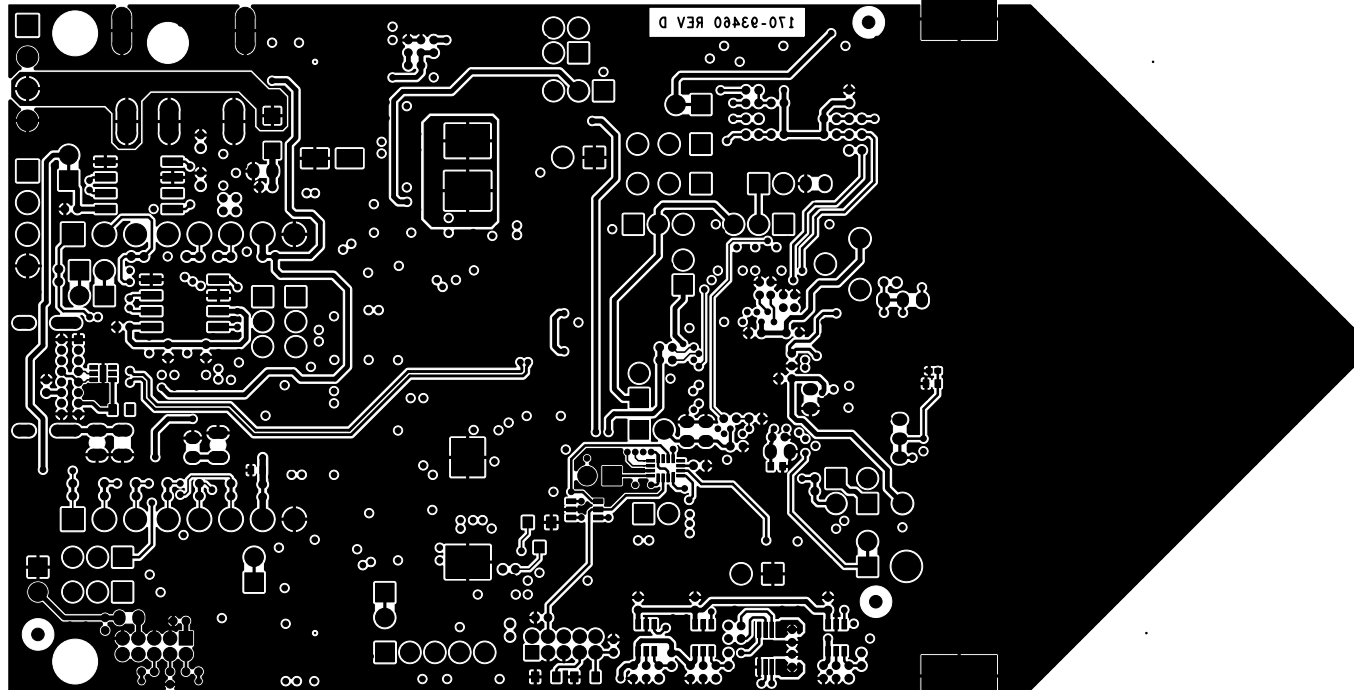
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SHEET 06 OF 12	FILM L3_INT_1	DATE 09-18-25	NUMBER 170-93460 REV D



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SHEET 08 OF 12	FILM L5_GND_2	DATE 09-18-25	NUMBER 170-93460 REV D



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SHEET 09 OF 12	FILM L6_SS	DATE 09-18-25	NUMBER 170-93460
		REV D	

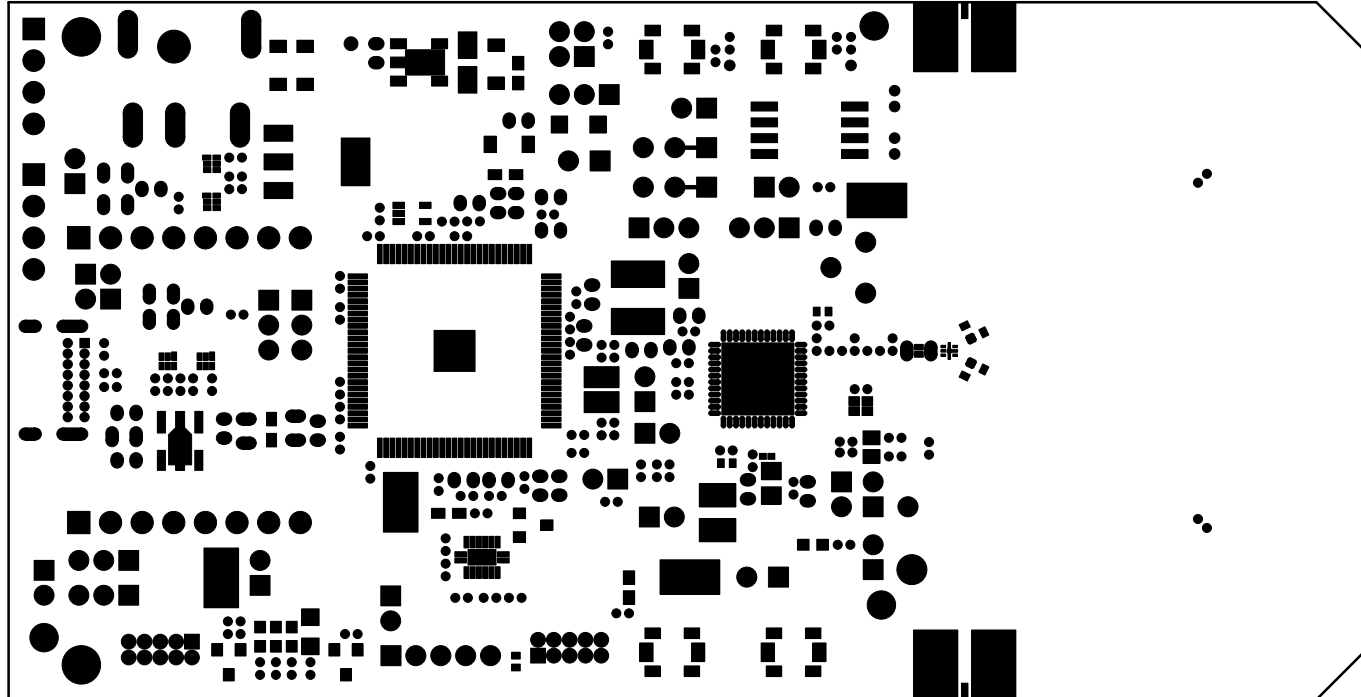


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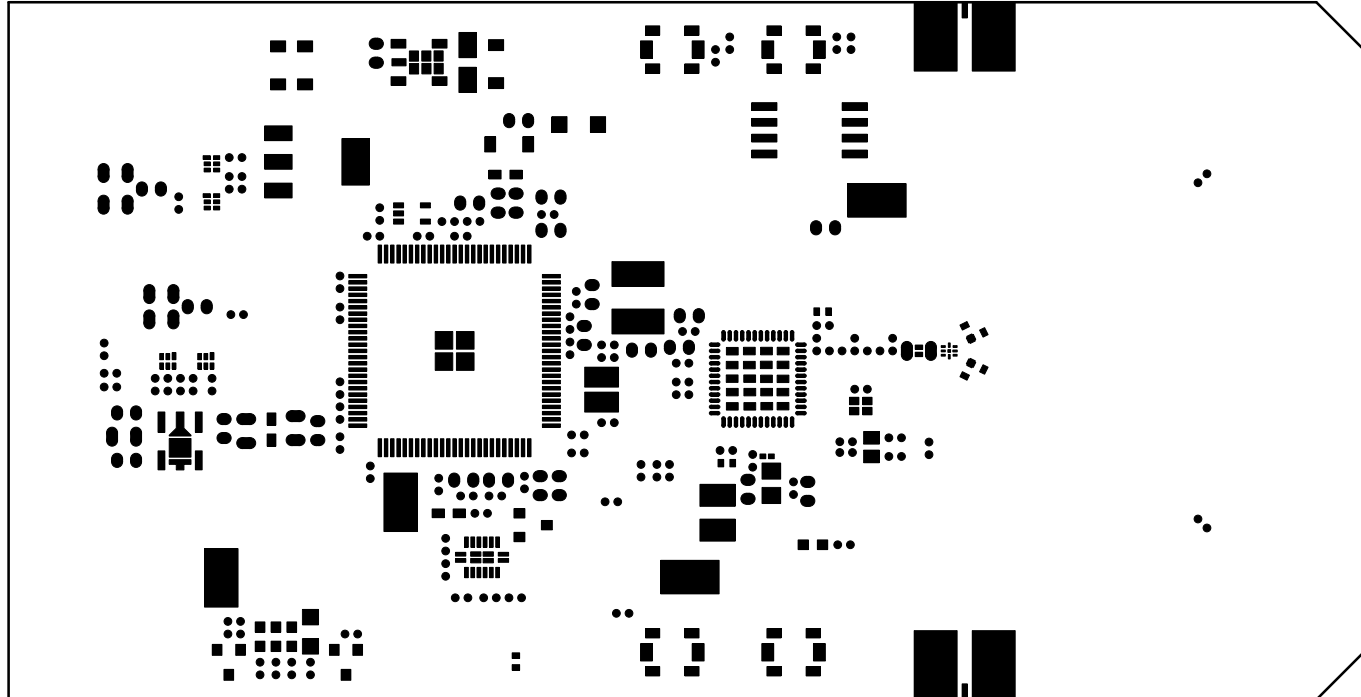
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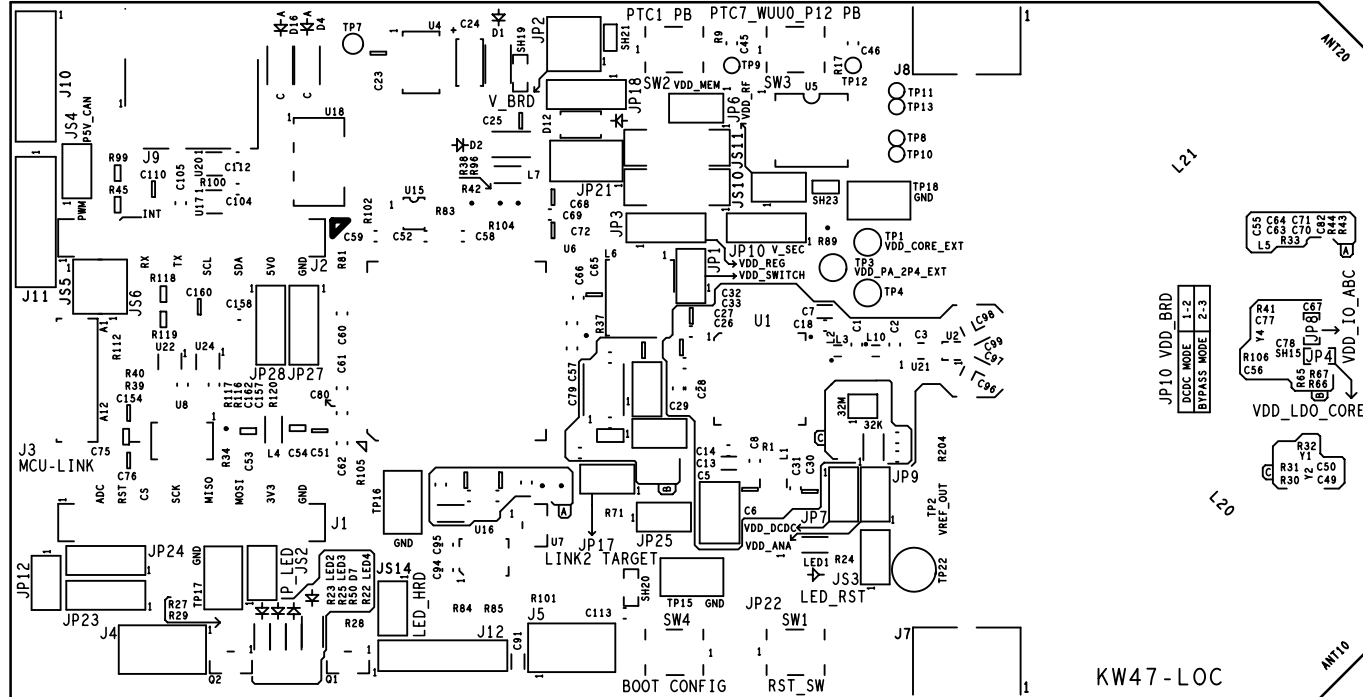
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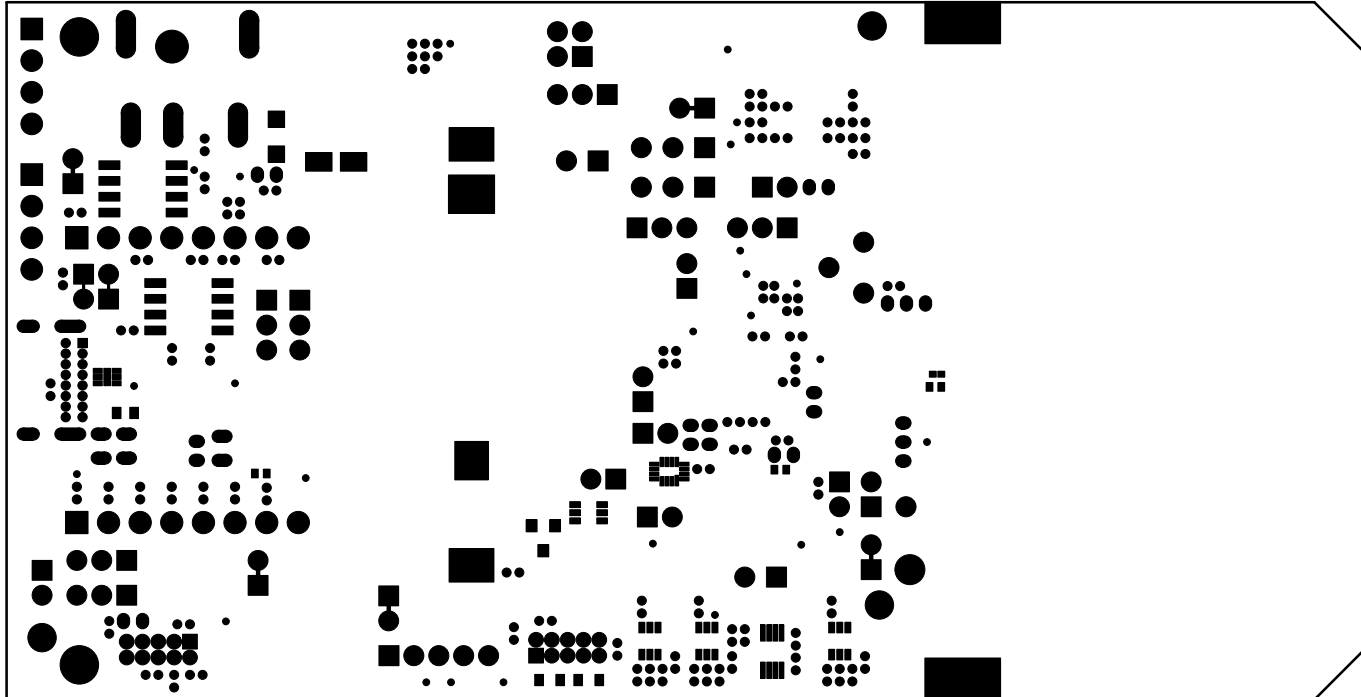
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SHEET 03 OF 12	FILM PRIMARY SOLDERMASK	DATE 09-18-25	NUMBER 170-93460 REV D



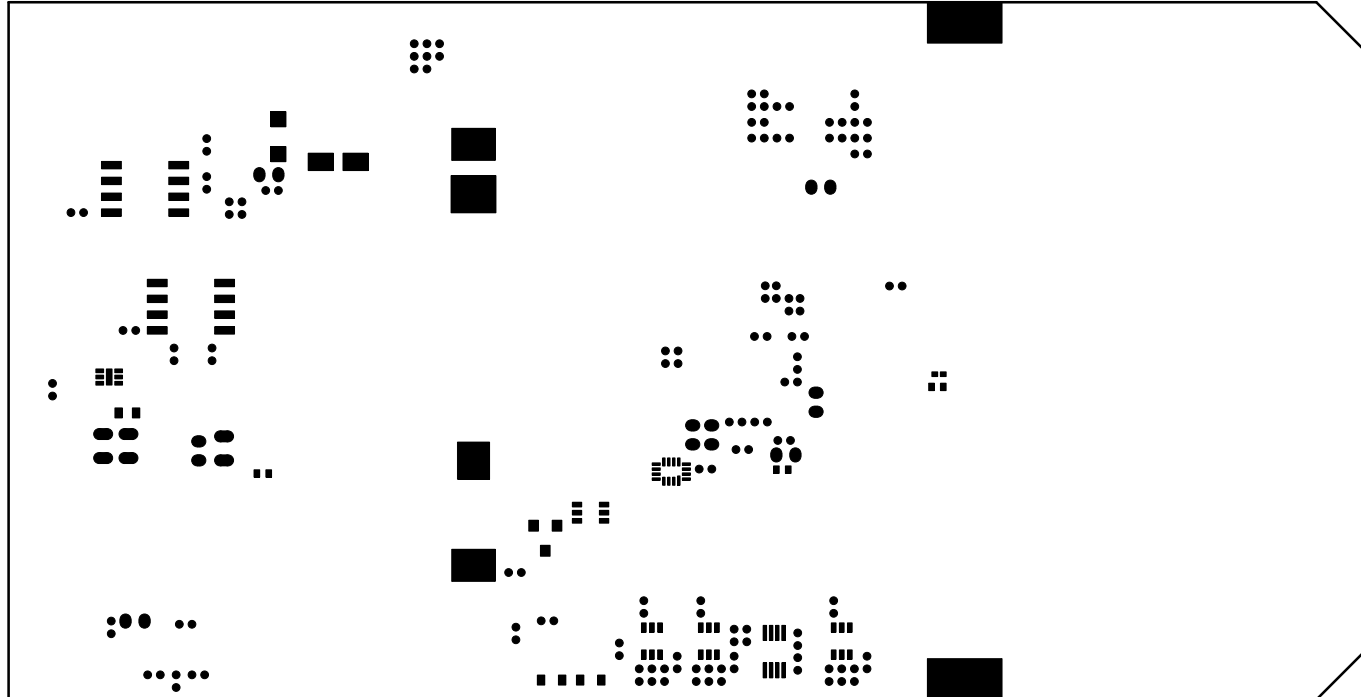
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SHEET 01 OF 12	FILM PRIMARY PASTEMASK	DATE 09-18-25	NUMBER 170-93460 REV D



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SHEET 02 OF 12	FILM PRIMARY SILKSCREEN	DATE 09-18-25	NUMBER 170-93460
		REV D	



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SHEET 10 OF 12	FILM SECONDARY SOLDERMASK	DATE 09-18-25	NUMBER 170-93460
		REV D	



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SHEET 12 OF 12	FILM SECONDARY PASTEMASK	DATE 09-18-25	NUMBER 170-93460 REV D

